IN THE CLAIMS:

Please cancel claims 18 and 19, without prejudice or disclaimer.

Please amend claim 17 as follows:

Sub B1 C1

17. A semiconductor device according to claim 2, wherein said first and second conductive layers are filled in first and second through-holes, and the upper ends thereof are connected to said first and second conductive layers, and the spatial intervals in the arrays of said first and second conductive layers are smaller than those in the arrays of said first and second through-holes.

REMARKS

Reconsideration of the above-identified application in view of the present amendment is respectfully requested. The applicants' acknowledge the careful consideration given to the present application by the Examiner. The present application has been amended as necessary to address the concerns raised by the Examiner.

By the present amendment the specification has been amended to correct the items identified by the Examiner in addition to several other items uncovered upon review of the specification.

A new title has been provided that is indicative of the invention to which the claims are directed.

Turning to the claims, claim 17 is amended and claims 18 and 19 are deleted. Accordingly, the issues raised with regard to the rejection of claims under 35 U.S.C. §112 are moot. Also, the issues raised with regard to the drawings are moot. However, it is to be appreciated that claims 18 and 19 are cancelled without prejudice and disclaimer such that these claims may be later presented in this or another

application with the understanding that these claims limitations are not relinquished.

Turning to the rejection of claims in view of cited documents, these rejections are respectively traversed. With regard to the rejection of claims in view of U.S. Patent No. 5,311,048 to Takahashi et al., it is to be noted that the Takahashi patent fails to provide all of the claim limitations provided in independent claim 1. Specifically, the Takahashi patent provides no discussion regarding capacitance permittivity, specific inductive capacitance, dielectric properties of any of the materials of the described device. Accordingly, it is wholly impossible that the Takahashi device has a distance between a first conductive layer and a second conductive layer that is determined in accordance with a permittivity of an insulating layer. To assert otherwise is to imbue teachings to the Takahashi patent that are just not present. Accordingly, all of the presently pending claims are allowable in view of the Takahashi patent.

Turning to U.S. Patent No. 4,954,877 to Nakanishi et al., it is noted that this patent is not a semiconductor device but is instead a carrier for a circuit chip that may be a semiconductor device. Accordingly, the Nakanishi patent fails to even be a device as set forth in the claims. As such, all of the pending claims are allowable over the Nakanishi patent.

Turning to U.S. Patent No. 5,598,029 to Suzuki, it is noted that this patent also fails to provide the present invention. The Office action identifies a first conductive layer 7a and second conductive layer 7b. However, the Suzuki patent, and the teachings provided therein, are directed to a bypass capacitor that is formed between a gate oxide film 3 and gate 4. The teaching regarding capacitance have nothing to do with the first and second conductive layers 7a and 7b. Further, there is no teaching within the Suzuki patent that is directed to permittivity of any insulating layer. To assert otherwise would be to imbue teachings to the Suzuki patent that are just not present. Accordingly, the Suzuki patent, as

interpreted within the Office action, necessarily fails to satisfy all of the limitations of the claims. Accordingly, all of the claims are allowable in view of the Suzuki patent.

In view of the forgoing, it is respectfully submitted that the above-identified application is in condition for allowance and allowance of the above-identified application is respectfully requested. If the Examiner is of the opinion that some issue remains that might prevent swift allowance of the subject application, the Examiner is invited to contact the applicants' representative via telephone.

If there are any fees required by the foregoing Amendment, please charge the same to our Deposit Account No. 16-0820, our Order No. 32811.

Respectfully submitted,
PEARNE & GORDON LLP

By: _____
Ronald M. Kachmarik, Reg. No. 34512

526 Superior Avenue East
Suite 1200
Cleveland, Ohio 44114-1484
(216) 579-1700

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VERSION SHOWING CHANGES MADE

IN THE TITLE:

The title as submitted was deleted and replaced as follows:

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME UTILIZING PERMITTIVITY OF AN INSULATING LAYER TO PROVIDE A DESIRED CROSS CONDUCTIVE LAYER CAPACITANCE PROPERTY

IN THE SPECIFICATION:

The paragraph on page 6, starting at line 19, was replaced with the following rewritten paragraph:

Preferably, said first conductive layer is [formed in] formed in a comb shape and said through-holes are formed at the positions sandwiched between the teeth of the comb.

The paragraph on page 19, starting at line 7, was replaced with the following rewritten paragraph:

Prior to explaining the modes of carrying out a semiconductor device and a method of manufacturing it according to the invention, consideration is taken on a change in the element structure (structure in the wiring layer or polysilicon layer) due to downsizing of the process technique. Figs. 2 and 3 are views for explaining the element structure constituting the corresponding portion of a semiconductor integrated circuit (polysilicon gate nMOS transistor). Fig. 3 shows the element structure by more advanced downsizing of the process than the case of Fig. 2. Fig. 2(a) and Fig. 3(a) are plan views (pattern views); Fig. 2(b) and Fig. 3(b) are sectional views taken in line A-A' in Fig. 2(a) and Fig. [2(b)] <u>3(a)</u>, respectively, and Fig. 2(c)and Fig. 3(c) are

sectional views taken in line B-B' in Fig. 2(a) and Fig. 2(c), respectively.

The paragraph on page 24, starting at line 18, was replaced with the following rewritten paragraph:

Further, the insulating inter-layer film can be made of a film having a high permittivity and the insulating inter-wiring film can be made of a film having a low permittivity. Thereby the capacitance between the through-holes and the capacitance between the wirings can be [epualized] equalized. Further by laminating a plurality of films having different film quality from each other, better dielectric characteristics can be obtained.

The paragraph on page 26, starting at line 4, was replaced with the following rewritten paragraph:

[hole]The through-holes B11 and B12 generally have a fixed square shape in section as shown in Fig. 1(a). However, where a supplemental capacitor is formed, since through-holes are formed on a semiconductor substrate, an insulating layer thereon or an insulating substrate, the problem such as fluctuation of etching does not occur. Therefore, the rule of the fixed shape of the through-hole may be disregarded so that the through-holes has a rectangular shape in section as shown in Fig. 1(c). Thereby an area of capacitor is increased and a large capacitance can be obtained. And by use of capacitance along a through hole depth direction, such a large capacitance can be obtained without increasing an occupied area.

The paragraph on page 29, starting at line 4, was replaced with the following rewritten paragraph:

Contrary that, in Fig.4(c), although the through-hole B43 being contacted with the poly-Si P41 has regular [squre] square form wiring, the through-holes B41, B42 used for

forming capacitors have a rectangular cross sections so as to increase an area facing to the poly-Si P41.

The paragraph on page 39, starting at line 19, was replaced with the following rewritten paragraph:

In Fig. 8, the poly-Si layer P81 has a planar shape formed along the respective side of an octagon so as to surround the through-hole B1. In the case that the poly-Si layer P81 has a regular [squre] square shape, a [destance] distance between the poly-Si layer P81 and the through-hole B81 at each edge portion of the regular [squre] square. Therefore according to the octagon shape, each edge portion of the regular [squre] square is made close to the through-hole B81. This shape can be realized in only a process rule in which the wiring of 45 degree on the skew of the right and left side is permitted. Where the wiring on the skew is not permitted, the planar shape of the poly-Si layer of P81 may be modified into the shape formed along the respective sides of a square. The planar shape of the poly-Si layer may be not the shape surrounding all the directions of the through-hole B81, but the shape partially surrounding the through-hole B81, e.g. [a ⊐-shape] an open-sided shape. In [the] this case, it is also preferable that inner edge of the poly-Si layer P81 is formed along the outer side of the though hole.

The paragraph on page 40, starting at line 23, was replaced with the following rewritten paragraph:

Moreover, in this embodiment, the various patterns of poly-Si layer formed along the respective sides of an octagon and a square and ["⊐-shape] open-sided shape may be registered as a single cell in a library of arranging/wiring tool (apparatus for assisting design of a semiconductor IC). Using these patterns alone or in combination, a supplemental capacitor having desired capacitance can be formed at a

desired position. This [is] can be applied to a semiconductor device with more regular arranging/wiring such as a gate array.

The paragraph on page 41, starting at line 19, was replaced with the following rewritten paragraph:

In Fig. 9, reference sign 901 denotes a Si substrate; B91m-B9jm and B91p-B9j+1p a through-hole; M92, M92 a metallic wiring; and P91-P9j+1 a poly-Si layer. The poly-Si layers P91-P9j+1 are connected to one another by the poly-Si layer shown in Fig. 9(a) under the metallic wiring M92. A spacer [411] 911 is formed on the side of each poly-Si layer and its side face and upper face are covered with an insulating protection film 912. Although not shown in Fig. 9(b), an insulating inter-layer film is formed around each of the through-holes B91m-B9jm.

The paragraph on page 42, starting at line 14, was replaced with the following rewritten paragraph:

In Fig. [4] 9, although the through-holes B91m-B9jm and poly-Si layer P91-P9j+1 were formed on the Si substrate 901, they may be formed on the insulating layer such an element isolation region of the Si substrate 901. Moreover, using an insulating substrate in place of the silicon substrate 901, this embodiment of the invention can be applied to a SOI (Silicon On Insulator) structure. This embodiment can also be applied to not only the MOS device but also the other device.

The paragraph on page 43, starting at line 9, was replaced with the following rewritten paragraph:

In Fig. 9, each of the through-holes B91m-B9jm is [surrounded like "⊐"] partially surrounded (e.g. on at least three of four sides) by the poly-Si layer. However, the pattern of the capacitor according to the second embodiment

may be successively arranged (i.e. there is no poly-Si under the metallic wiring M91 in Fig. 9). Moreover, in this embodiment, the various patterns of the poly-Si layer such as ["⊐"-shape and "="-shape] a three-sided partially surrounding shape and a two-sided partially surrounding shape may be registered as a single cell in a library of arranging/wiring tool (apparatus for assisting design of a semiconductor IC). Using these patterns in successive combination, a supplemental capacitor having desired capacitance can be formed at a desired position. This [is] can be applied to a semiconductor device with more regular arranging/wiring such as a gate array.

The paragraph on page 46, starting at line 12, was replaced with the following rewritten paragraph:

The structure as shown in Fig. 7 can be manufactured in the same manner as in the second embodiment, and can be realized at least in the following process. First, in a step of forming an electrode layer, poly-Si layers P101, P102 are formed on a Si substrate 1001. Next, in a step of forming an insulating protective film, a spacer 1011 is formed on the side of each of the poly-Si layers P101, P102 and an insulating protective film 1012 is formed to cover it. In a step of forming an insulating inter-layer film, the insulating inter-layer if formed. In a step of forming a through-hole, the insulating inter-layer film is etched to form a [though-holes] through-holes B101, B102. Further, in a step of forming a wiring, metallic wirings M101 and M102 are formed on the through-holes B101 and B102. Since the poly-Si layers are formed with high processing accuracy, the supplemental capacitor having an accurate capacitance can be formed.

IN THE CLAIMS:

Claims 18 and 19 were cancelled without prejudice or disclaimer.

Claim 17 was amended as follows:

17. (amended) A semiconductor device according to claim 2, wherein said first and second conductive layers are filled in [said] first and second through-holes, and the upper ends thereof are connected to said first and second conductive layers, and the spatial intervals in the arrays of said first and second conductive layers are smaller than those in the arrays of said first and second through-holes.